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Washington, D.C. 20231

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22 November 2000

INTELLECTUAL PROPERTY LAW

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☐ Via E-Mail Attachment
☐ Please Acknowledge Receipt

Attorney Docket: P56257

Sir:

Submitted herewith is the following patent application:

Inventor: WOO-JONG PARK

**Title: ADDRESS SEARCH APPARATUS AND METHOD IN
ETHERNET SWITCH**

Please find attached hereto an application for patent which includes: Specification and Abstract,
Claims, original Declaration And Power of Attorney, Assignment, and a certified copy of the
foreign priority document identified below:

Verified Showing of Small Entity Status: **NO**

Drawings: Formal drawings, 6 sheets, Figures 1 through 6

Claim of priority under 35 U.S.C. §119: **YES**

** The Republic Of Korea Application No. 51825/1999 filed on 22 November 1999

FEE (see formula below): CHECKS ARE ENCLOSED (## 37705, 37706)

Basic Fee \$345/690 **\$710.00**

Additional Fees:

Total number of claims in excess of 20: ____ times \$9/18 . **\$0.00**

Number of independent claims in excess of 3: ____ times \$40/80 **\$0.00**

Multiple Dependent Claims \$130/260 **\$0.00**

An Assignment is likewise enclosed: Recording Fee \$40 . . **\$40.00**

Filing Non-English specification **\$0.00**

TOTAL FEES FOR THE ABOVE APPLICATION \$750.00

Assistant Commissioner for Patents
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Page Two

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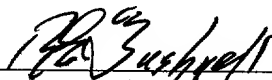
Assistant Commissioner is authorized to charge our Deposit Account No. 02-4943 for any additional charges necessary towards payment of the issue fee for the above-referenced application. Please notify the undersigned attorney of any transaction regarding our Deposit Account.

In view of the above, it is requested that this application be accorded a filing date pursuant to 37 CFR 1.53(b).

Please address all correspondence to:

Robert E. Bushnell
1522 K Street, N.W.
Suite 300
Washington, D.C. 20005

Respectfully submitted,



Robert E. Bushnell
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REB/kf

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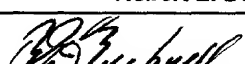


FEE TRANSMITTAL

Patent fees are subject to annual revision.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PTO/SB/17 (08-00)
Approved for use through 9/30/2000. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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SUBMITTED BY Typed or Printed Name: <u>Robert E. Bushnell, Esq.</u> Signature:  Date: <u>22 November 2000</u>		Complete (if applicable) Reg. Number: <u>27,774</u> Deposit Account User ID: _____																																																																																																																																																																																																																																																							

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WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

TITLE OF THE INVENTION

ADDRESS SEARCH APPARATUS AND METHOD IN ETHERNET SWITCH

CLAIM OF PRIORITY

This application makes reference to, incorporates the same herein, and claims all benefits accruing under 35 U.S.C. §119 from my application *ADDRESS SEARCH APPARATUS AND METHOD IN ETHERNET SWITCH* filed with the Korean Industrial Property Office on 22 November 1999 and there duly assigned Serial No. 51825/1999.

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to a data network, and more particularly an apparatus and a method for performing an efficient address search in a switch network.

Description of the Related Art

Ethernet is a most typical protocol of LAN(Local Area Network) which occupies a very important portion in data networks. Ethernet is widely accepted in the industry already, and the application thereof reaches all kinds of data networks. At the present, since users are rapidly increasing and more various services are getting provided, bandwidth of a network is required to be wider than before. Providing wide bandwidth of a network enables converting from a repeater so called hub into a switch in a remarkably rapid speed. As compared to a repeater which shares a

1 transmission medium, a switch efficiently uses only required sources from transmission means to
2 receiver means thereby having a very rapid transmission speed.

3 Herein, "address search" means that an ethernet switch establishes required information to
4 determine an output terminal, and collects and utilizes information for address. The address search
5 is particularly important in an application in which management for address is highly required.
6 Examples of the application include ARP(Address Resolution Protocol) management,
7 NMS(Network Management System), RMON(Remote Monitoring) and etc.

8 In an example of an address searching method in an ethernet switch as shown in FIG. 1, a
9 search memory interface(SMI) 6 receives a header and a port number of an input packet from a
10 PCU(Port Control Unit) in each of port devices 2-0, 2-1, ..., 2-7 to establish data about source
11 address on a search memory, and determines an output port of each packet on the basis of the
12 establish data.

13 However, in Fig. 1, since the 8 port devices are required to determine output ports by using
14 the same search unit, the input packet of one port (device) only can be searched while the remaining
15 ports (devices) are left to wait. Also, there are some structural problems in realizing a search logic
16 required for a management switch, i.e., a switch which has a control unit for controlling an ethernet
17 switch when the switch structure is a non-management switch, i.e. a switch which does not have a
18 control unit for controlling an ethernet switch. An interface for sharing address data with other units
19 was not defined also. In other words, in the non-management switch structure, the address structure
20 is not suitably realized for a management switch.

SUMMARY OF THE INVENTION

Therefore, it is an object of the present invention to provide an improved ethernet switch and switching process.

It is also an object of the present invention to provide an apparatus and a method for performing an efficient address search operation in an ethernet switch network.

It is another object of the present invention to provide an apparatus and a method in which conversion from a non-management switch structure into a management structure or a port expansion is easy.

According to the foregoing objects of the present invention, it is provided with a processing structure in which a number of ports use one search unit, said structure having a local search block corresponding to each of the ports to perform a search operation as a distributed processing structure.

It is also provided with a structure in which an information exchange between the local search blocks and a main search block for port and a search operation on individual addresses can be proceeded without an error.

Furthermore, it is provided with an address search apparatus in an ethernet switch having a plurality of ports, having a local search unit corresponding to each of the plurality of ports; wherein the local search unit includes: a plurality of local search blocks for analyzing a destination address of an input packet received in the port thereof to search for a transmission port of the ethernet switch and provide a source address thereof; a main search unit for analyzing the source address to establish an address data structure of the plurality of local search blocks, and for responding to a destination address request from at least one of the plurality of local search blocks to provide the requested

1 destination address to a corresponding local search block by using the address data structure; and a
2 scheduler for controlling the local search blocks and the main search unit to enable an interface
3 therebetween.

4 BRIEF DESCRIPTION OF THE DRAWINGS

5 A more complete appreciation of the invention, and many of the attendant advantages thereof,
6 will be readily apparent as the same becomes better understood by reference to the following detailed
7 description when considered in conjunction with the accompanying drawings in which like reference
8 symbols indicate the same or similar components, wherein:

9 FIG. 1 is a view for showing an address searching method in an ethernet switch;

10 FIG. 2 is a view for showing an address searching method in an ethernet switch according
11 to an embodiment of the present invention;

12 FIG. 3 is a detailed block diagram for showing one of local search blocks shown in FIG. 2;

13 FIG. 4 is a detailed block diagram of a main search block shown in FIG. 2;

14 FIG. 5 is a message format diagram for an interface between search blocks according to an
15 embodiment of the present invention; and

16 FIG. 6 is a flow chart illustrating how an incoming packet of information is sent to a
17 destination port according to an embodiment of the present invention.

18 DETAILED DESCRIPTION OF THE INVENTION

19 Referring to FIG. 1 in more detail, each of the port devices 2-0, 2-1, ..., 2-7, which

corresponds to each of ports 0, 1, ..., 7 for example, includes a physical hierarchy unit for functioning as a physical hierarchy, a MAC(Medium Access Control) unit for functioning as a medium access control, and a PCU(Port Control Unit). When a packet is received by at least one port at random, some of the port devices 2-0, 2-1, ..., 2-7 of the ports corresponding to the received packet, output control signal command availables(cmd_avl) to a scheduler 4, respectively. When receiving control signal cmd_avl, the scheduler 4 which is periodically operated controls one port to be selected via competition and enables an address search about the selected one port (device). In other words, when receiving the control cmd_avl, the scheduler 4 schedules a priority set on the basis of a predetermined control or a port selection order on the basis of a round robin, and provides a resultant port selection signal to both of a multiplexer(MUX) 10 and a demultiplexer(DEMUX) 12. The predetermined control can be set by users for example. The multiplexer 10 selects one from 8 port devices 2-0, 2-1, ..., 2-7) in response to the port selection signal provided by the scheduler 4, and receives a header and a port number from the selected port device to output to search memory interface 6. The header can include destination address, source address, and etc. Then, the search memory interface 6 establishes data about the source address on the search memory 8, and determines an output port corresponding to the selected input packets on the basis of the established data. After determining the output port, the search memory interface 6 outputs the determined information to the corresponding one of the 8 port devices 2-0, 2-1, ..., 2-7 via the demultiplexer 12. After that, the search memory interface 6 outputs a control signal cmd_cpl which notifies completion of output port determination to the scheduler 4.

FIG. 2 is a view for showing an address searching method in an ethernet switch according

to an embodiment of the present invention. Referring to FIG. 2, an address searching apparatus according to an embodiment of the present invention includes 8 local search blocks 20-0, 20-1, ..., 20-7, for example, and one main search block 26, in which an interface protocol is defined for information exchange between the local search blocks 20-0, 20-1, ..., 20-7 and the main search block 26. Each of the 8 local search blocks 20-0, 20-1, ..., 20-7 is arranged to correspond to each of 8 port devices 22-0, 22-1, ..., 22-7 arranged within the ethernet switch, and the main search block 26 is arranged between the scheduler 24 and a search memory (not shown in FIG. 2). Each of the 8 local search blocks 20-0, 20-1, ..., 20-7 analyzes a destination address of an input packet received in a port thereof to search for a transmission port of the ethernet switch, and the main search block 26 analyzes the destination address to establish an address data structure of the local search blocks. When transmitting and receiving data, the scheduler 24 which is periodically operated permits a port to be selected from the plurality of ports and interfaces control signals between the local search blocks 20-0, 20-1, ..., 20-7 and the main search block 26.

FIG. 3 is a detailed block diagram for showing one of local search blocks 20-0, 20-1, ..., 20-7 shown in FIG. 2. Referring to FIG. 3, each of the local search blocks 20-0, 20-1, ..., 20-7 has 2 address tables, i.e., a destination address table 30 and a source address table 32. In the destination address table 30, destination address and destination information (such as transmission port numbers) are matched. In the source address table 32, source addresses and source information (such as input port numbers) are matched. Also, address sorting logics 34 and 36 corresponding to the destination address table 30 and the source address table 32 respectively are arranged to sort an ethernet address into groups as many as necessary. Each of the local search blocks 20-0, 20-1, ..., 20-

7 has a control logic 38 for controlling the corresponding search block and a register unit 40 for temporal storage of data.

FIG. 4 is a detailed block diagram of the main search block 26 shown in FIG. 2. The main search block 26 includes an address table 50, a table access logic 48, an address sorting logic 46, a control logic 42, and a register unit 44. The address table 50 is a memory for storing addresses known to a system. In using the memory, a hash function (“/”) is used to satisfy characteristics of the ethernet address. The hash function can be subdivided according to methods for obtaining hash keys, in which a method using XOR gate(exclusive OR gate) is adapted in an embodiment of the present invention. The table access logic 48 is a kind of access logic for accessing the address table 50 structured as above. The table access logic 48 performs the foregoing hash function. Therefore, when the individual addresses are searched, desired information stored in the address table 50 can be obtained via the table access logic 48. The address sorting logic 46 is a logical function block for classifying addresses having same characteristics in order to store data known to the system into the address table 50. The control logic 42 and the register unit 44 have blocks, i.e., an external processor and an interface for controlling each of these blocks according to functions and for determining conditions thereof. Also, the control logic 42 and the register unit 44 exchange information via an interface between the local search blocks 20-0, 20-1, ..., 20-7 corresponding to each of the port device 22-0, 22-1, ..., 22-7, and construct each address table.

FIG. 5 is a message format diagram for an interface between the search blocks according to the embodiment of the present invention. Referring to FIG. 5, messages include a command field CMD, an ID field(identifier field), and a specification information field according to the CMD

1 information. In the command field CMD, commands(CMD) such as search, add, delete and update
2 can be recorded, and the ID field includes a transmitter ID for transmitting the messages of FIG. 5
3 and a receiver ID for receiving the messages. For example, when transmitting messages from the
4 local search block 20-0 to the main search block 26, the transmitter ID will be the ID of the local
5 search block 20-0 and the receiver ID will be the ID of the main search block 26. The specification
6 information field according to the CMD information includes specification information according
7 to the CMD information. The CMD information may include search, add, delete, update and etc. as
8 described above, and the resultant specification information may include MAC address, header
9 information of a packet, port ID, device number, input port number and etc. The header information
10 of a packet includes source and destination addresses.

11 Hereinafter, operations for address search according to the embodiment of the present
12 invention will be described in more detail in reference to FIG. 2 to FIG. 5 in conjunction with FIG.
13 6. When a packet is received (Step 100) in a certain port device 22-N (herein, N is one of 0 to 7) of
14 the 8 port devices 22-0, 22-1, ..., 22-7, the local search block 20-N corresponding to the port device
15 22-N reads a destination address from a header information (Step 105) of the packet to compare with
16 the destination addresses in the destination address table 30 (Step 110). The foregoing comparing
17 is performed by the address sorting logic 34. The address sorting logic 34 performs address sorting,
18 i.e., an operation for classifying an ethernet address into groups as many as necessary, thereby more
19 easily accessing the internal destination table 30. An example of algorithms for classifying into
20 groups may include a hash algorithm. When the destination address of the input packet exists in the
21 address table 30, the control logic 38 of the local search block 20-N obtains a required information

(Step 115), i.e., a destination information (transmission port). After that, the local search block 20-N rejects the input packet via filtering when the destination information (transmission port) is proved to be its own port (Step 125). Describing the above in more detail, when obtaining the destination information (transmission port), the address sorting logic 36 compares the source addresses in the source address table 32 with the destination address of the input packet (Step 120). When the destination address of the input packet exists in the source address table 32, the input packet is rejected by filtering (Step 125). In other words, the packet is proved that transmission to other port is not required, and then filtered. In turn, when the destination information (transmission port) obtained from the destination address table 30 is not identical with the destination address of the input packet in the source address table 32, or when the destination information (transmission port) obtained from the destination address table 30 is a different port, the address sorting logic 36 provides the corresponding information to the corresponding port device 22-N.

In turn, when the destination address of the input packet does not exist in the address table 30 in the local search block 20-N (Step 110), the address sorting logic 36 receives a corresponding destination address from the main search block 26 to update the destination address table 30 in the local search block 20-N. Describing the above in more detail, the local search block 20-N sends a message loaded with a search command in the command field CMD, a source ID and a destination ID in the identifier field ID, and header information of the packet in the specification information field according to the CMD information to the main search block 26 (Step 130), according to the protocol defined between the local search blocks 20-0, ..., 20-7 and the main search block 26. Then, the main search block 26 performs an internal search (Step 135) about the destination address in the

received header information, and when the address search is successfully completed, transmits an information about the searched destination address to the corresponding local search block 20-N. Then, the corresponding local search block 20-N transmits the destination information (transmission port) received from the main search block 26 to the corresponding port device 22-N thereby permitting the port device 22-N to transmit the input packet (Step 160), and updates the table information of the destination address table 30 (Step 155) in the local search block 20-N at the same time. If an information of the corresponding destination address (hereinafter referred to "port information") does not exist in the main search block 26 in addition to being found in the local search block, the main search block 26 sends a no-port information of the destination to the corresponding local search block 20-N (Step 145) since the port information about the address does not exist in the present system. When the corresponding local search block 20-N receives the no-port information, the corresponding port device 22-N performs a forwarding operation. The forwarding operation means broadcasting (Step 150). In other words, since it is not determined to which port the input packet is required to be transmitted, the packet is transmitted to all available ports (except input ports) in the ethernet switch. In turn, the local search blocks 20-0, 20-1, ..., 20-7 corresponding to the ports respectively and the main search block 26 periodically perform an update operation of the source and destination addresses.

Hereinafter, the operation will be described in detail. The local search blocks 20-0, 20-1, ..., 20-7 corresponding to the ports respectively periodically transmit header information (such as source addresses, destination addresses and etc.) to the main search block 26 so that the main search block 26 can perform an address update (Steps 143 & 157). The main search block 26 establishes an

address data structure via address learning via input of the header information (such as source addresses, destination addresses and etc.) transmitted from the local search blocks 20-0, 20-1, ..., 20-7 which correspond to the ports respectively. In other words, the information used for establishing the address data are port information of the sub hosts of the system and addresses allocated thereto. This information can be obtained since each of the hosts causes its address information to be included in the header of the packet while transmitting and receiving the packets. The information corresponding to the source address, as though it may be varied according to objects to which the system is aimed, can be supposed simply as a port information in the system (i.e., as to which port the source address corresponds).

Describing the address learning process in more detail, the main search block 26 searches whether a corresponding information (such as address information, port information and etc.) exists in the address table 50 of the main search block 26 about the destination and source addresses. When a corresponding information exists, the main search block 26 performs an information update operation desired by the system including an address aging. Herein, the address aging means clearing old address data, i.e. address data which are not used for a predetermined period, from the addresses stored in the address table 50 of the main search block 26 (Step 157). Performing the information operation including the address aging like this can establish new information as address data. When a corresponding information does not exist, the address learning operation is performed. The address learning is generally performed by an external processor, and data insertion is carried out into the link structure by using hash within the main search block 26 (Step 143). In other words, the search information (such as MAC address, port number and add command) connected in respect to the

corresponding source address is provided by the external processor, but actual operation to connect data to the link according to the hash key is carried out in the main search block 26.

In turn, the local search block 20-N requests port information of the destination and source addresses to the main search block 26 when the destination and source addresses of the input packets do not exist in the destination table 30 and the source address table 32 of the local search block 20-N. Then, the main search block 26 provides port information of the requested destination address and source addresses to the local search block 20-N so that the local search block 20-N may update the destination and source addresses and corresponding port information in the destination address table 30 and the source address table 32.

As described above, the invention can reduce required time in a large amount by managing a small table for each port than search operation which are carried out via competition while sharing single search logic. Therefore, the main search block can carry out more tasks. Also, exchange of address information with other system can be carried out by conversion into a management switch structure or a port expansion, and the overall search efficiency can be enhanced by management of suitable table by each port.

While the invention has been described in detail by specific reference to preferred embodiments thereof such as an ethernet switch, it is understood that variations and modifications thereof may be made without departing from the true spirit and scope of the invention. In other words, the variations and modifications can be made to a switch network which include at least one of packet switch, asynchronous transfer mode (ATM) network and etc. Therefore, it should be understood that the true spirit and the scope of the invention are not limited by the above

embodiment, but defined by the appended claims and the equivalents thereof.

WHAT IS CLAIMED IS:

1. An address search apparatus in an ethernet switch, said apparatus comprising:

a plurality of ports;

a plurality of local search blocks corresponding to each of said plurality of ports, said plurality of local search blocks for analyzing a destination address of an input packet received in the port thereof to search for a transmission port of said ethernet switch and provide a source address thereof;

a main search unit for analyzing said source address to establish an address data structure of said plurality of local search blocks, and for responding to a destination address request from at least one of said plurality of local search blocks to provide said requested destination address to a corresponding local search block by using said address data structure; and

a scheduler for controlling said local search blocks and said main search unit to enable an interface therebetween.

2. The address search apparatus according to claim 1, each of said plurality of local search blocks includes:

a destination address table having destination addresses and destination information corresponding to said destination addresses which are matched therein;

a source address table having source addresses and source information corresponding to said source addresses which are matched therein;

an address sorting logic for classifying an ethernet address into groups as many as necessary,
and corresponding to each of said destination address table and said source address table;
a control logic for control of corresponding local search blocks; and
a register unit for temporal storage of data.

3.The address search apparatus according to claim 1, said main search unit includes:

an address table for storing addresses known to the ethernet switch system and port
information corresponding to said addresses;
a table access logic for accessing said address table;
an address sorting logic for classifying addresses having same characteristics to store data
known to the ethernet switch system into said address table; and
a control unit for control and condition detection of elements.

4.An address search method in use for an address search apparatus in an ethernet switch, said
address search method comprising the steps of:

providing a plurality of ports, a local search unit corresponding to each of said plurality of
ports for local address search and a main search unit for overall address search of the ethernet switch;
judging whether the corresponding local search unit has a destination port information
corresponding to the destination address by using a destination address of a packet received in one
of the plurality ports; and
requesting for a destination port information corresponding to the destination address to the

main search unit when the local search unit does not have the destination port information.

5. An address search method in an ethernet switch, said method comprising the steps of:
determining whether or not a port has received an information packet for transmission;
reading a destination address from a header of said information packet;
determining whether said destination address exists in a local search block of said port;
determining whether said destination address is the same as a source address; and
transmitting said information packet to said destination address if said destination address
is in said local search block of said port and is not the same as said source address.

6. The method of claim 5, further comprising the step of rejecting said information packet
if said destination address is the same as said source address.

7. The method of claim 5, further comprising the steps of:
notifying a main search block if said destination address is not found in said local search
block of said port;
performing an internal search by said main search block to find said destination address;
updating said local search block of said destination address if said main search block
comprises said destination address; and
transmitting said information packet to said destination address.

1 8. The method of claim 7, further comprising the steps of:

2 sending no-port information from said main search block to said port device if said main

3 search block does not comprise said destination address; and

4 broadcasting said information packet to all ports in said ethernet switch by said port device.

1 9. The method of claim 7, further comprising the step of aging, wherein said main search

2 block purges addresses that have not recently been used.

1 10. The method of claim 8, further comprising the step of address learning, wherein said

2 main search block adds said destination address to its address table.

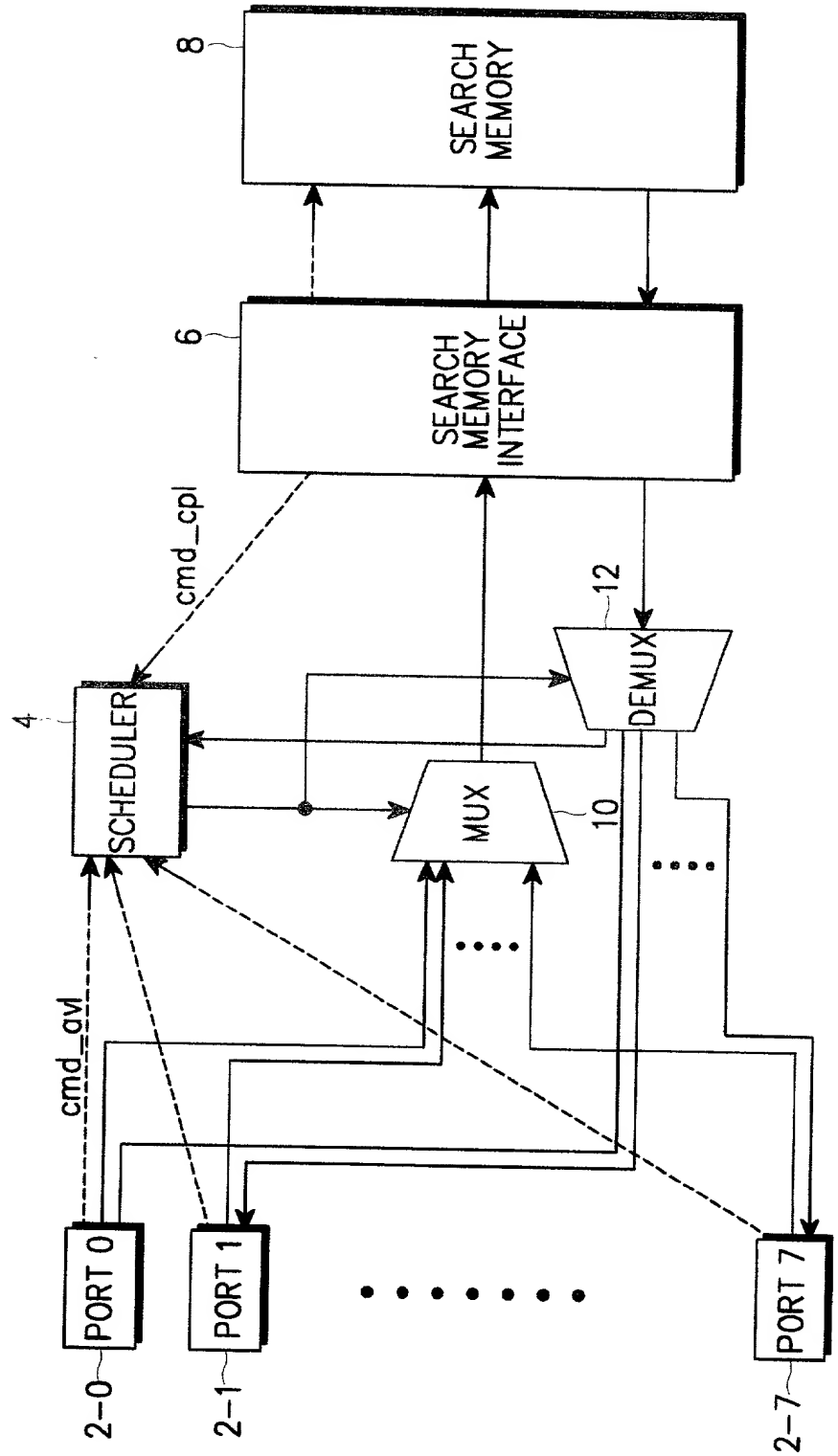
1 11. The method of claim 10, further comprising the step of adding said destination address

2 to said local search block.

ABSTRACT OF THE DISCLOSURE

An apparatus and a method for performing an efficient address search in an ethernet switch having a plurality of ports, said apparatus having a local search unit corresponding to each of the plurality of ports; wherein the local search unit includes: a plurality of local search blocks for analyzing a destination address of an input packet received in the port thereof to search for a transmission port of the ethernet switch and provide a source address thereof; a main search unit for analyzing the source address to establish an address data structure of the plurality of local search blocks, and for responding to a destination address request from at least one of the plurality of local search blocks to provide the requested destination address to a corresponding local search block by using the address data structure; and a scheduler for controlling the local search blocks and the main search unit to enable an interface therebetween.

FIG. 1



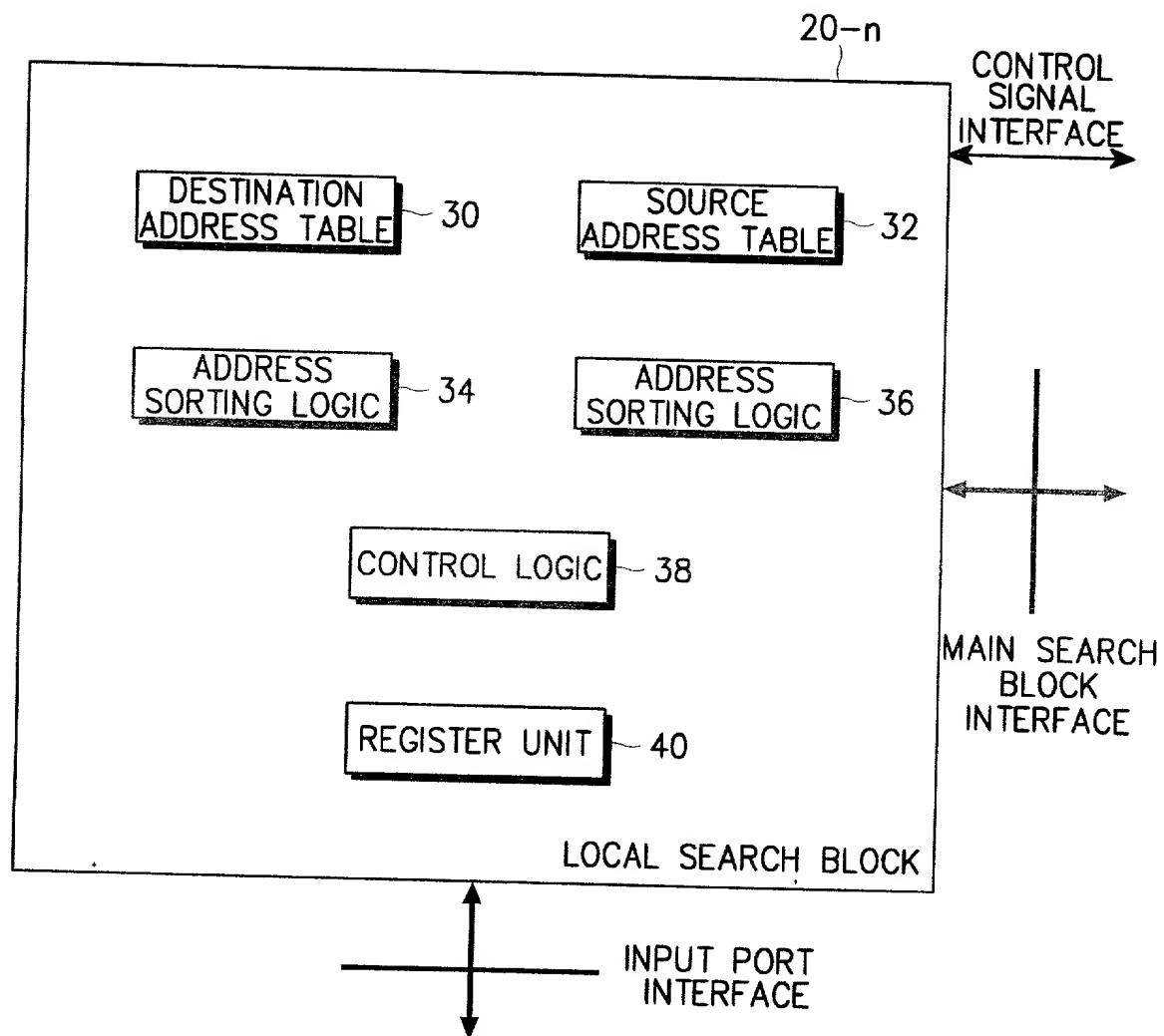
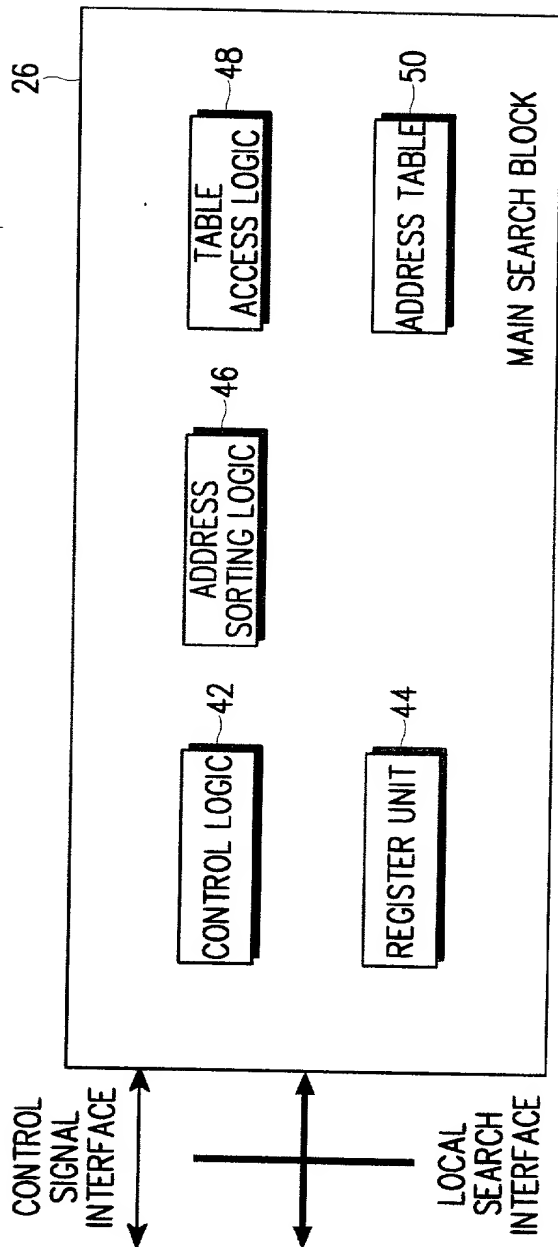


FIG. 3

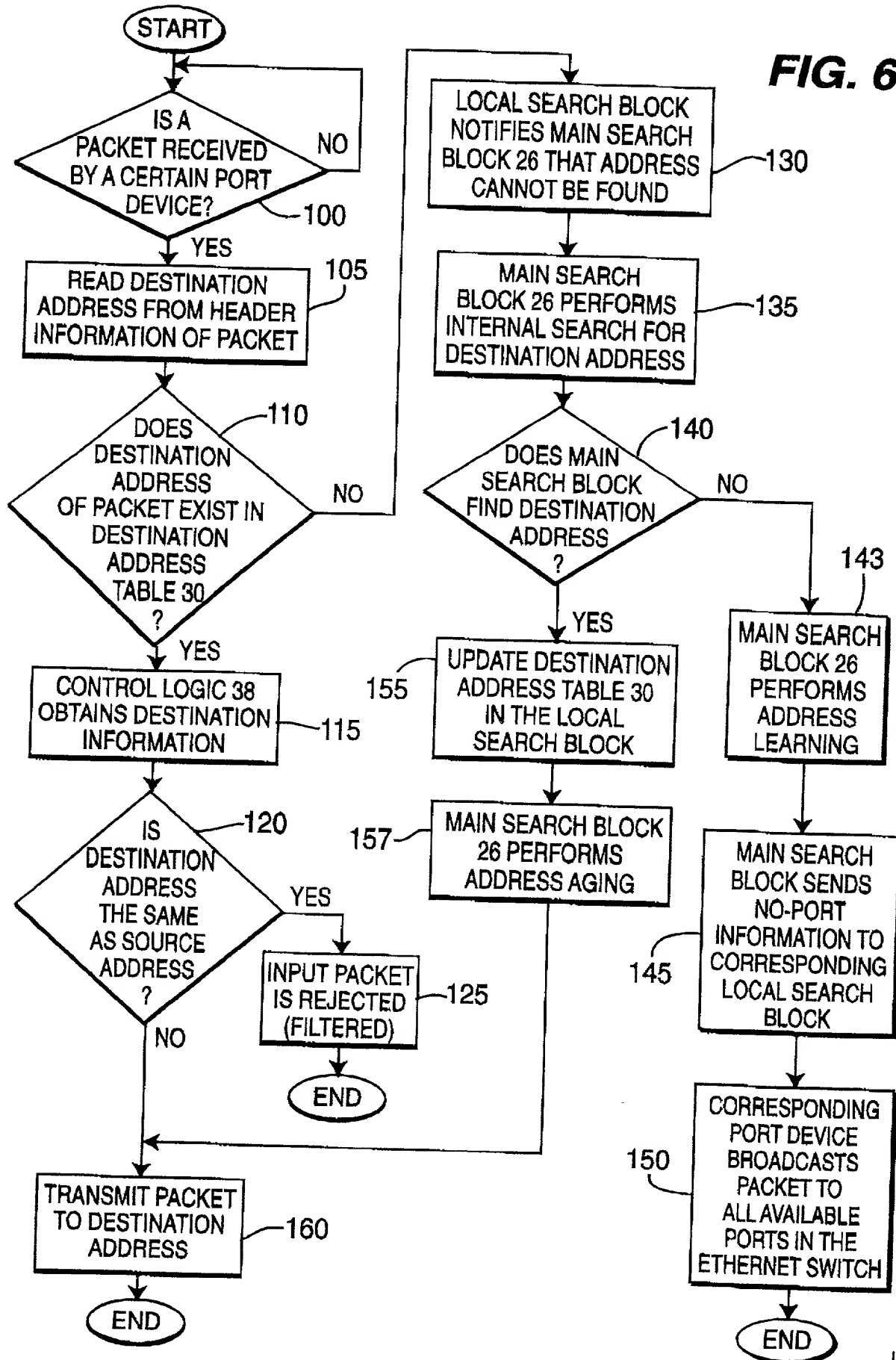
FIG. 4



CMD	ID
SPECIFICATION INFORMATION ACCORDING TO CMD INFORMATION	

FIG. 5

FIG. 6



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

WOO-JONG PARK

Serial No.: *to be assigned*

Examiner: *to be assigned*

Filed: 22 November 2000

Art Unit: *to be assigned*

For: ADDRESS SEARCH APPARATUS AND METHOD IN ETHERNET SWITCH

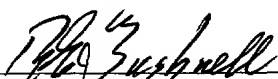
TRANSMITTAL OF DECLARATION

Assistant Commissioner
for Patents
Washington, D.C. 20231

Sir:

This transmittal accompanies the original Declaration for the above-referenced application.

Respectfully submitted,



Robert E. Bushnell,
Attorney for the Applicant
Registration No.: 27,774

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Folio: P56257
Date: 11/22/00
I.D.: REB/kf

DECLARATION

Docket No.

P56257

AS A BELOW NAMED INVENTOR, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole (if only one name is listed below), or an original, first and joint inventor (if plural names are listed below), of the subject matter which is claimed and for which a patent is sought on the invention entitled:

TITLE: "ADDRESS SEARCH APPARATUS AND METHOD IN ETHERNET SWITCH"

the specification of which either is attached hereto or otherwise accompanies this Declaration, or:

was filed in the U.S. Patent & Trademark Office on _____ and assigned Serial No. _____

and (if applicable) was amended on _____

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability and to the examination of this application in accordance with Title 37 of the Code of Federal Regulations §1.56. I hereby claim foreign priority benefit under Title 35, U.S. Code §119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States, or §119(e) of any United States provisional application(s), listed below and have also identified below any foreign applications for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

(Application Number)	(Country)	(Day/Month/Year filed)
1049-51825	Republic of Korea	27/11/1999

Priority Claimed:
Yes [X] No []

Yes [] No []

I hereby claim the benefit under Title 35, U.S. Code, §120, of any United States application(s), or §365(a) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application(s) in the manner provided by the first paragraph of Title 35, U.S. Code, §112, I acknowledge the duty to disclose information material to patentability as defined in Title 37, The Code of Federal Regulations, §1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(STATUS: patented, pending, abandoned)

I hereby revoke all previously granted powers of attorney and appoint the following attorneys: Robert E. Bushnell, Reg. No. 27,774, Michael D. Parker, Reg. No. 34,973, and Darren R. Crow, Reg. No. 37,806, to prosecute this application and to transact all business in the U.S. Patent & Trademark Office connected therewith and with any divisional, continuation, continuation-in-part, reissue or re-examination application, with full power of appointment and with full power to substitute an associate attorney or agent, and to receive all patents which may issue thereon, and request that all correspondence be addressed to:

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Attorney-at-Law
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Phone No. 008439
Area Code: 202-408-9040

I HEREBY DECLARE that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 U.S. Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's signature: _____ Date: November 21, 20
Residence & Post Office Address: Hwanggol Jugong APT. #152-1202, Maejin-dong, Paldal-gu, Suwon-shi, Kyonggi-do, Republic of Korea

FULL NAME OF SECOND JOINT INVENTOR: _____ Citizenship: _____
Inventor's signature: _____ Date: _____
Residence & Post Office Address: _____

FULL NAME OF THIRD JOINT INVENTOR: _____ Citizenship: _____
Inventor's signature: _____ Date: _____
Residence & Post Office Address: _____

FULL NAME OF FOURTH JOINT INVENTOR: _____ Citizenship: _____
Inventor's signature: _____ Date: _____
Residence & Post Office Address: _____

If Additional inventors are being named on separately numbered sheets attached hereto.